

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D. Remarks

To address this ground for rejection, Applicant's establish invention of the subject matter of claims 1, 2, and 25 prior to the effective date of *Yoshihara et al.* (see the attached "Declaration Under 37 C.F.R. §131" and supporting Disclosure Document with translation).

This submission includes additional portions of the Disclosure Document. Invention of the subject matter of claims 1, 2 and 25 is established by the following:

1. The written description on pages 3 and 4 of the interoffice document.
2. The figures shown in Section 8.1 of the interoffice document. Applicant has attached an enlarged version of these figures in Exhibit C. English translations of the Kanji/Kana labels are shown in this example. These translations are readily evident from the text of Pages 3 and 4 and corresponding translation.

A direct correspondence between the figures of the disclosure document, and Applicant's Application Figures is as follows:

Applicant's Figure	Corresponding Figure in Section 8.1 of Interoffice Document of Exhibits A, B, C
FIG. 2(a)	First Column From Left: (a)
FIG. 2(b)	First Column From Left: (b)
FIG. 2(c)	First Column From Left: (c)
FIG. 3(d)	First Column From Left: (d)
FIG. 3(e)	First Column From Left: (e)
FIG. 3(f)	First Column From Left: (f)
FIG. 5(a)	Second Column From Left: (a)
FIG. 5(b)	Second Column From Left: (b)
FIG. 5(c)	Second Column From Left: (c)
FIG. 6(d)	Second Column From Left: (d)
FIG. 6(e)	Second Column From Left: (e)
FIG. 6(f)	Second Column From Left: (f)

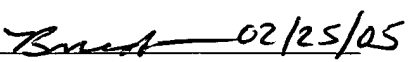
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FIG. 7(g)	Second Column From Left: (d)
FIG. 7(h)	Second Column From Left: (e)
FIG. 7(i)	Second Column From Left: (f)
FIG. 9(a)	Third Column From Left: (e)
FIG. 9(b)	Third Column From Left: (f)
FIG. 9(c)	Third Column From Left: (g)
FIG. 10	Third Column From Left: (h)
FIG. 12(a)	Fourth Column From Left: (d)
FIG. 12(b)	Fourth Column From Left: (e)
FIG. 12(c)	Fourth Column From Left: (f)
FIG. 13(d)	Fourth Column From Left: (g)
FIG. 13(e)	Fourth Column From Left: (h)
FIG. 13(f)	Fourth Column From Left: (i)

The present claims 1-2 and 25 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

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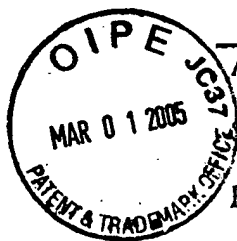
Respectfully Submitted,


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Reg. No. 37,923

10

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicant(s): Satoh, Yoshihiro

Serial No.: 09/981,402

Filed: October 17, 2001

Title: Semiconductor Device and Method
for Its Manufacture

Attorney Docket No.: N32040200W

Group Art Unit: 2815

Examiner: Richards, N. D.

DECLARATION UNDER 37 C.F.R. §1.131 by ASSIGNEE

5 Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

10 I, Takeo Fujii, representing Elpida Memory, Inc., do hereby declare and
state:

1. After a diligent effort, the inventor for this patent application was not available to
15 produce a declaration to swear behind the present reference.

2. Prior to October 12, 2000, a semiconductor device and structure on a silicon
substrate as described and claimed in this patent application was conceived. Disclosure of the
invention is shown in the communication dated August 9, 2000 (see Exhibits A and B).

20 3. On October 20, 2000 a patent application for the invention was filed in Japan, a
WTO member country.

25 4. On October 17, 2001 this patent application, based on the Japanese Patent
Application, was filed in the U.S.

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I hereby declare that all statements made herein are true and with the knowledge that willful false statements and like so made are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code.

Signed:

Takeo Fujii

Name: Takeo Fujii

Date _____

for Elpida Memory, Inc.

10

Executive Manager
Intellectual Property Gr.
Finance & Legal Office

15

Rule 131 Declaration

BEST AVAILABLE COPY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

EXHIBIT A

DISCLOSURE DOCUMENTS IN SUPPORT OF
DECLARATION UNDER 37 C.F.R. §1.131

For Serial No.: 09/981,402
Applicant(s): SATOH, Yoshihiro

アイデア提案書		事業部整理番号: 744-10431	
提案日: 2000年 8月 9日		グループコード: 4J600 部内番号: _____	
[承認欄] 部長: _____ 課長: _____ 主任: _____		半特許受付日: _____	
[提案者記入欄]		E-mail: y-satou@eu.jp.nec.com	
提案者所属: 1メモリ デバイス設計部			
提案者氏名: 佐藤 好弘		社員番号: _____	
適用・応用分野: 半導体装置の構造および製造方法			
適用製品名: _____		売上規模: _____ (百万円/年)	
実験・試作状況: <input type="radio"/> 実験・試作完了 <input checked="" type="radio"/> 実験・試作中 <input type="radio"/> 実験・試作予定あり <input type="radio"/> 実験・試作予定なし			
先行特許調査(調査した中で近い特許公開番号): _____			
先行文献調査(調査した中で近い公知例): _____			
特許検索式: _____			
関連提案・特許: _____			
サンプル出荷/社外発表予定: <input checked="" type="radio"/> 無 <input type="radio"/> 有(早い方の日: _____)			
出願希望種別: <input type="radio"/> コンカレント <input type="radio"/> OS級 <input checked="" type="radio"/> 通常出願			
[発明相談コメント欄] 8/11 センター担当: _____ 年 月 日			
[証人署名欄]			
本提案書(図面を含む)の第1ページから第 _____ ページを読んで発明内容を理解しました。			
氏名: 堀 端 信一 2000年8月9日			
[発明者署名欄]			
氏名: 佐藤 好弘 2000年8月9日			
氏名: _____ 20 年 月 日			

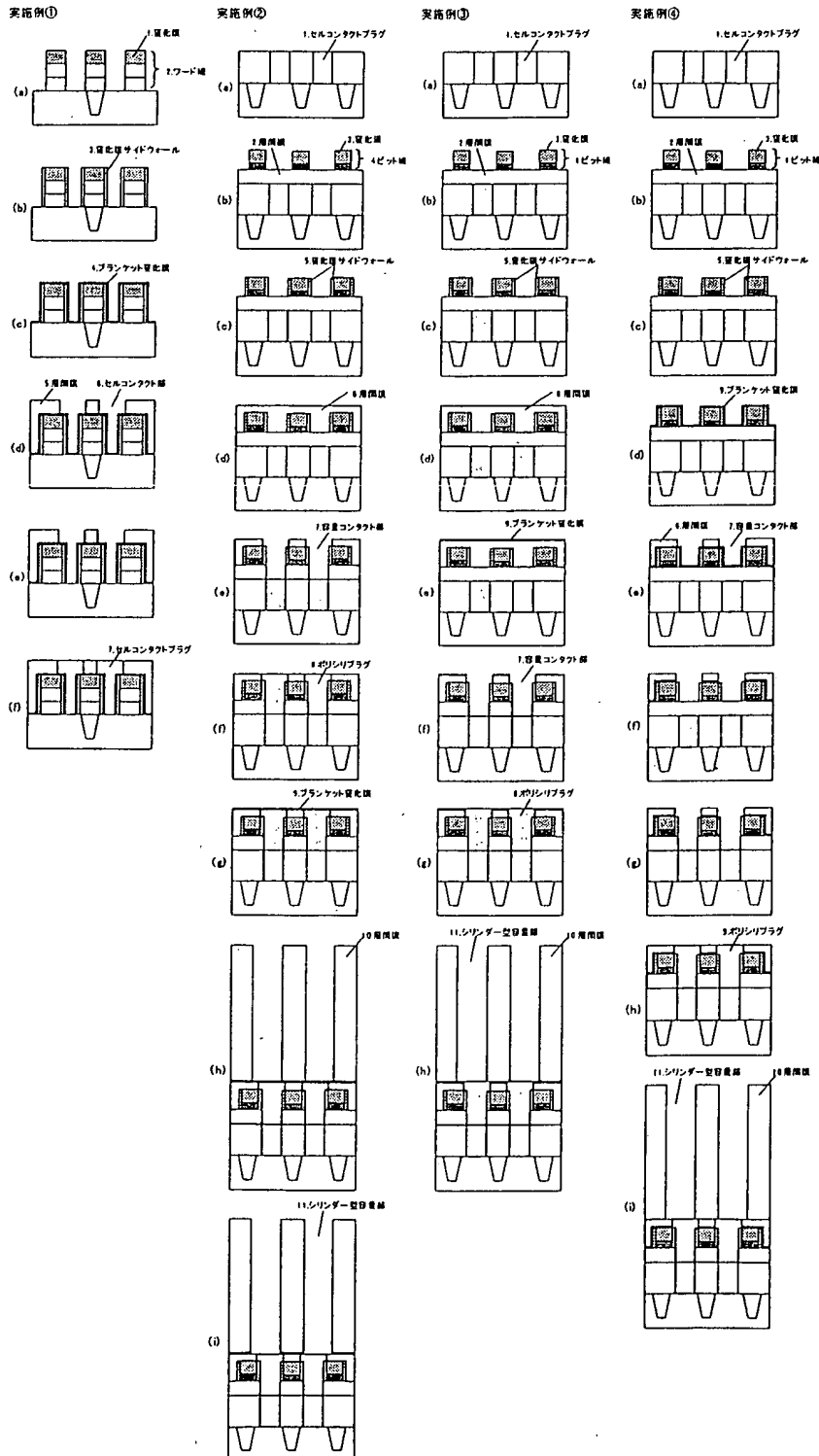
1. 【発明の名称】

半導体装置の構造および製造方法

2. 【発明の特徴】

容量絶縁膜にタンタルオキไซด์(Ta₂O₅)を用いた場合のDRAMにおいて、その有機系原材料に含まれるカーボンの拡散を防止するための膜として、シリコン基板と容量絶縁膜の間に窒化膜で構成されるストッパー膜を形成する。

8. 1【発明の図】



3. 1[発明の構成と動作、製法と手順等]

①シリコン基板上に窒化膜1を用いたワード線2を形成した後、その上層に窒化膜を形成し、エッチバックすることにより、ゲートの側壁に窒化膜サイドウォール3を形成する。次に、カーボンの拡散防止膜として、ブランケット窒化膜4を形成する。その後、層間膜5を形成し、ゲート間を埋設する。その後、レジストマスクパターンなどを用い、窒化膜と選択比のあるエッチングにより、ブランケット窒化膜4までエッチングし、セルコンタクト部6を形成する。次に、窒化膜をエッチバックすることにより、セルコンタクト部6の窒化膜を除去し、その後、セルコンタクトプラグ7を形成する。

②ワード線(図示せず)を形成した後、拡散層上に容量と接続されるセルコンタクトプラグ1を形成する。次に、層間膜2を形成し、その上層に窒化膜3を用いたビット線4を形成する。その後、窒化膜をエッチバックすることにより、ビット線の側壁に窒化膜サイドウォール5を形成する。さらに、ビット線間を層間膜6で埋設し、レジストマスクパターンなどを用い、窒化膜と選択比のあるエッチングにより容量コンタクト部7を形成し、その後ポリシリプラグ8を形成する。その上層にカーボンの拡散防止膜として、ブランケット窒化膜9を形成する。その後はシリンダー型容量形成のための層間膜10を形成し、レジストマスクパターンなどを用い、最初に窒化膜と選択比のあるエッチングによりブランケット窒化膜9までエッチングし、次に酸化膜と選択比あるエッチングによりブランケット窒化膜9のみをエッチングし、シリンダー型容量部11を形成する。

③窒化膜を用いたビット線4を形成した後、その上層に窒化膜を形成し、エッチバックすることにより、ビット線の側壁に窒化膜サイドウォール5を形成する。さらに、ビット線間を層間膜6で埋設し、その上層にカーボンの拡散防止膜として、ブランケット窒化膜9を形成する。その後、レジストマスクパターンなどを用い、ブランケット窒化膜9および層間膜6をエッチングし、容量コンタクト部7を形成し、その後ポリシリプラグ8を形成する。その後はシリンダー型容量形成のための層間膜10を形成し、レジストマスクパターンなどを用い、エッチングによりシリンダー型容量部11を形成する。

④窒化膜を用いたビット線4を形成した後、その上層に窒化膜を形成し、エッチバックすることにより、ビット線の側壁に窒化膜サイドウォール5を形成する。次に、カーボンの拡散防止膜としてブランケット窒化膜9を形成し、ビット線間を層間膜6で埋設し、レジストマスクパターンなどを用い、窒化膜と選択比のあるエッチングによりブランケット窒化膜9までエッチングし、容量コンタクト部7を形成する。次に、窒化膜をエッチバックすることにより、容量コンタクト部のブランケット窒化膜9を除去する。さらに、窒化膜と選択比のあるエッチングにより、セルコンタクトプラグ1まで、容量コンタクト部7を形成する。その後はポリシリプラグ8を形成し、その上層にシリンダー型容量形成のための層間膜10を形成し、レジストマスクパターンなどを用い、エッチングによりシリンダー型容量部11を形成する。

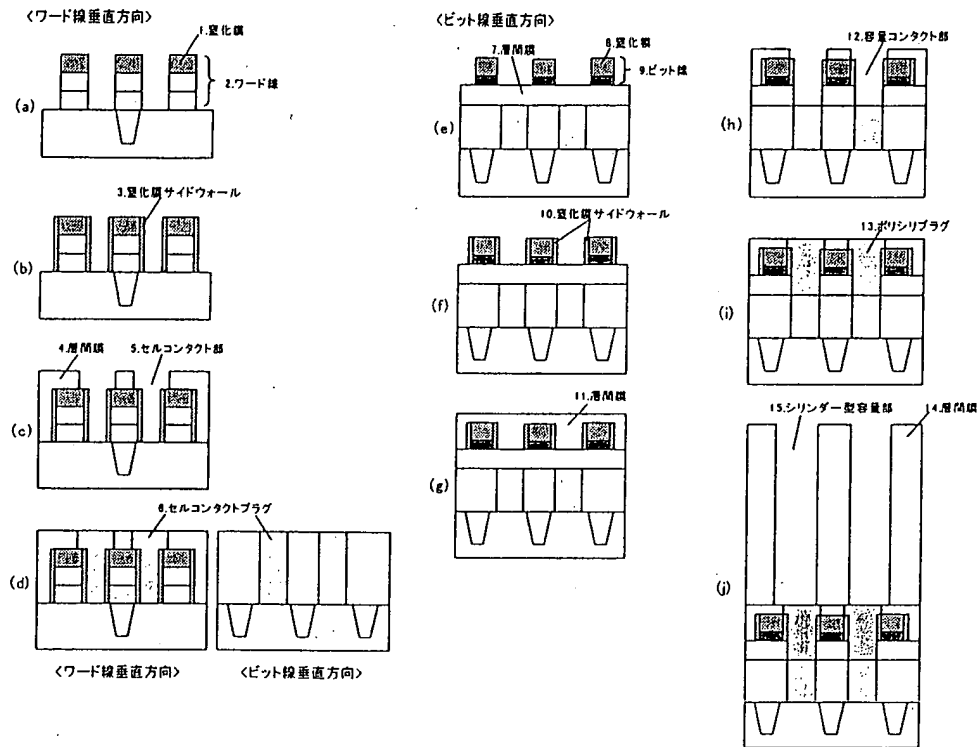
3. 2[発明の主な効果]

窒化膜で構成される層を容量絶縁膜とシリコン基板との間に形成することにより、容量絶縁膜にタンタルオキシサイド(Ta_2O_5)を用いた場合にその原材料に含まれるカーボンの拡散を防止することができ、トランジスタのハンプ特性および閾値変動などデバイス設計上問題視される悪影響を除外できる。

3. 3[上記効果が得られる理由]

容量絶縁膜とシリコン基板の間に窒化膜が形成されているため、カーボンの拡散が妨げられるため。

8. 2[従来の図]



5. 1[従来の構成と動作、製法と手順等]

シリコン基板上に窒化膜1を用いたワード線2を形成した後、その上層に窒化膜を形成し、エッチバックすることにより、ゲートの側壁に窒化膜サイドウォール3を形成する。次に、層間膜4を形成し、ワード線間を埋設した後、レジストマスクパターンなどを用い、窒化膜と選択比のあるエッチングにより、セルコンタクト部5を形成し、その後、セルコンタクトプラグ6を形成する。さらに、その上層に層間膜7を形成した後、窒化膜8を用いたビット線9を形成する。その後、窒化膜をエッチバックすることにより、ビット線の側壁に窒化膜サイドウォール10を形成する。ビット線間を層間膜11で埋設した後、レジストマスクパターンなどを用い、窒化膜と選択比のあるエッチングにより容量コンタクト部12を形成し、その後ポリシリプラグ13を形成する。その上層にシリンドー型容量形成のための層間膜14を形成し、レジストマスクパターンなどを用いエッチングし、シリンドー型容量部15を形成する。

5. 2[従来の主な欠点]

容量絶縁膜とシリコン基板との間に窒化膜の層が形成されていないため、容量絶縁膜にタンタルオキサイド(Ta_2O_5)を用いた場合、カーボンがシリコン基板まで拡散し、トランジスタの特性変動を引き起こす要因となる。

5. 3[上記欠点を生じる理由]

容量絶縁膜とシリコン基板との間に窒化膜の層が形成されていないため。

6. 【権利範囲】

容量絶縁膜とシリコン基板との間に窒化膜の層が形成されていることを特徴とする。

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

EXHIBIT B

Translation of Disclosure Document of EXHIBIT A

IN SUPPORT OF DECLARATION UNDER 37 C.F.R. §1.131

For Serial No.: 09/981,402
Applicant(s): SATOH, Yoshihiro

(4th Edition: 1998.02.25)		Body Page 1 of 4
Idea proposal	Business Unit Management Number: 744-10431	
Date of proposal: Aug 9, 2000	Group code: 4J600	Section Internal Number:
[Approval] Director:		Received: (Seal of Aug. 21, 2000 Intellectual Property Section: Ukai)
<p>[Items filled in by the proposer]</p> <p>e-mail: y-satou@eu.jp.nec.com</p> <p>Section where the proposer belongs: Memory Device Design 1,</p> <p>Name of the proposer: Yoshihiro Sato Employee Number:</p> <p>Application field: construction and manufacturing method of a semiconductor device</p> <p>Applied product name: Sales amount: (million Yen/year)</p> <p>Experiment/prototyping status: <input type="checkbox"/> experiment/prototyping done <input type="checkbox"/> experimenting/prototyping <input type="checkbox"/> experiment/prototyping planned <input type="checkbox"/> experiment/prototyping not planned</p> <p>Preceding patent research (close Patent publication number in the research):</p> <p>Preceding reference research (close known example in the research):</p> <p>Patent search:</p> <p>Related proposal/patent:</p> <p>Sample shipment/presentation schedule outside company: <input type="checkbox"/> none <input type="checkbox"/> yes (earlier date: year month day, where)</p> <p>Application type requested: <input type="checkbox"/> Concurrent <input type="checkbox"/> S class <input type="checkbox"/> Normal application</p>		
<p>[Invention Consulting comment] Person in charge at the Center: Date:</p>		

[Witness signature]

I have read the proposal (including figures) from Page 1 to Page and understood the content of the invention.

Name: Shinichi Horiba Date: August 9, 2000

[Inventor signature]

Name: Yoshihiro Sato Date: August 9, 2000

Name: Date:

1. [Name of the invention]

Construction and manufacturing method of a semiconductor device

2. [Characteristics of the invention]

For DRAMs in which tantalum oxide (Ta_2O_5) is used for the capacitance insulation film, a stopper film that consists of a nitride film is formed between the silicon substrate and the capacitance insulation film to prevent the diffusion of carbon contained in the organic materials.

8.1 [Figures of the invention]

(Figures: Small characters are illegible even after enlargement)

3.1 [Construction and operation, manufacturing method, and procedures, etc. of the invention]

1. After forming word lines 2 using a nitride film on the silicon substrate, another nitride film is formed on it, and nitride sidewalls 8 are formed on the sidewalls of the gate by etching back the film. Next, as a carbon diffusion prevention film, a blanket nitride film 4 is formed. Afterward, an interlayer film 5 is formed filling in between the gates.

Afterward using a resist mask pattern etc. combined with a nitride film selective etching method, the film is etched back to the blanket nitride film 4 exposing the cell contact area

6. Next, by etching back the nitride film, the nitride film of the cell contact area is removed, creating the cell contact plug 7.

2. After forming the word lines (not shown in the figure), the cell contact plug 1 that is to be connected to the capacitance is formed on the diffusion layer. Next, the interlayer film 2 is formed, and bit lines 4 are formed upon this using the nitride film 8. Afterward, by etching back the nitride film, the nitride film sidewalls 5 are formed on the sidewalls of the bit lines. Further, filling in between the bit lines with interlayer film 6, using a resist mask pattern etc. combined with a nitride film selective etching method, the capacitance contact area 7 is created, and then the poly-sili plugs 8 are formed. Next, as a carbon diffusion prevention film, a blanket nitride film 9 is formed on this. Afterward, an interlayer film 10 is formed to create a cylindrical capacitance. Using a resist mask pattern etc. first combined with a nitride film selective etching method, etching is performed to the blanket nitride film 9, and secondly combined with an oxide film selective etching method, only the blanket nitride film is etched, creating a cylindrical capacitance area 11.

3. After forming bit lines 4 using a nitride film, another nitride film is formed on it and by etching back the film, nitride sidewalls 5 are formed on the sidewalls of the bit lines. Further, filling in between the bit lines with the interlayer film 6, and as a carbon diffusion prevention film, the blanket nitride film 9 is formed. Afterward, using a resist mask pattern etc. both the blanket nitride film 9 and the interlayer film 6 are etched creating the capacitance contact area 7, and then poly-sili plug 8 is formed. Afterward, the interlayer film 10 is formed to create the cylindrical capacitance, and using a resist mask pattern etc. the cylindrical capacitance area 11 is created by etching.

4. After forming the bit lines 4 using a nitride film, another nitride film is formed on it, and the nitride sidewalls 5 are formed on the sidewalls of the bit lines by etching back the film. Next, as a carbon diffusion prevention film, the blanket nitride film 9 is formed, filling in between the bit lines with the interlayer film 6, and using a resist mask pattern etc. combined with a nitride film selective etching method, the film is etched back to the blanket nitride film 9 exposing the cell contact area 7. Next, by etching back the nitride film, the blanket nitride film 9 of the capacitance contact area is removed. Further, using a

nitride film selective etching method, the capacitance contact area 7 is created to the cell contact plug 1. Further, poly-sili plug 8 is formed, and the interlayer film 10 is formed to create the cylindrical capacitance, and using a resist mask pattern etc. the cylindrical capacitance area 11 is created by etching.

3.2 [Main effects of the invention]

By creating a layer consisting of a nitride film between the capacitance insulation film and the silicon substrate, diffusion of carbon contained in the material when tantalum oxide (Ta_2O_5) is used can be prevented, which results in the removal of unwanted troublesome affects on designing devices such as hump characteristics and threshold value fluctuation of transistors.

3.3 [Reason for the above effects]

Diffusion of carbon is prevented as the nitride film is formed between the capacitance insulation film and the silicon substrate.

8.2 [Figures for previous construction]

(figures)

5.1 [Previous construction and operation, manufacturing method, and procedures, etc.]

After forming word lines 2 using a nitride film 1 on the silicon substrate, another nitride film is formed on it, and nitride sidewalls 3 are formed on the sidewalls of the gate by etching back the film. Next, an interlayer film 4 is formed, filling in between the word lines, and using a resist mask pattern etc. combined with a nitride film selective etching method, the cell contact area 5 is created and then the cell contact plug 6 is formed. Next, by etching back the nitride film, the nitride film sidewalls 10 are formed on the sidewalls of the bit lines. After filling in between the bit lines with the interlayer film 11, using a resist mask pattern etc. combined with a nitride selective etching method, the capacitance contact area 12 is formed, and then the poly-sili plug 13 is formed. Upon this, the interlayer film 14 is formed to create the cylindrical capacitance, and using a resist mask pattern etc. the cylindrical capacitance area 15 is created by etching.

5.2 [Major defects of the conventional construction]

As there is no nitride film layer between the capacitance insulation film and the silicon substrate, carbon is diffused to the silicon substrate when tantalum oxide (Ta_2O_5) is used for the capacitance insulation film, causing characteristic fluctuation of the transistor.

5.3 [Reasons for the above defects]

Because a nitride film layer is not formed between the capacitance insulation film and the silicon substrate.

5. [Range of right]

It is characterized by the formation of nitride film layer between the capacitance insulation film and the silicon substrate.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

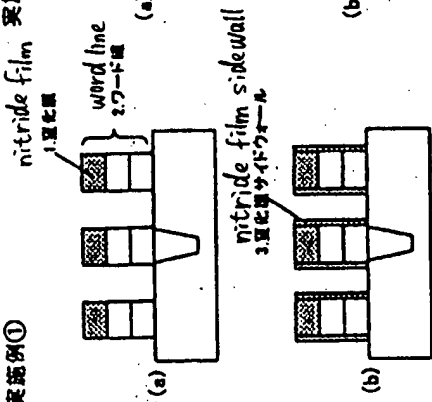
EXHIBIT C

ENLARGED AND DOCUMENTED FIGURES FROM DISCLOSURE DOCUMENTS
IN SUPPORT OF
DECLARATION UNDER 37 C.F.R. §1.131

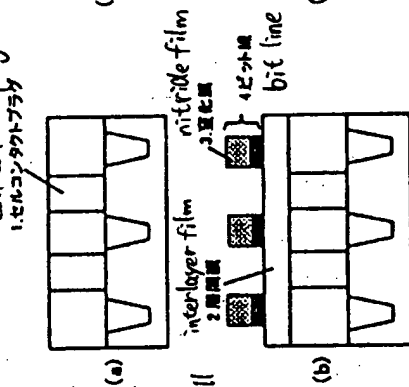
For Serial No.: 09/981,402
Applicant(s): SATOH, Yoshihiro

8.1【発明の図】

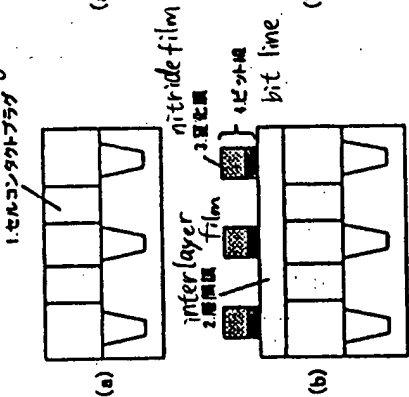
实施例①



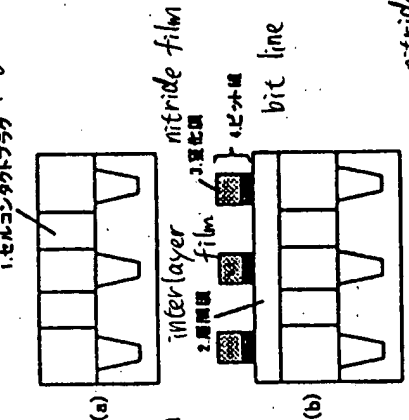
实施例②



cell contact plug

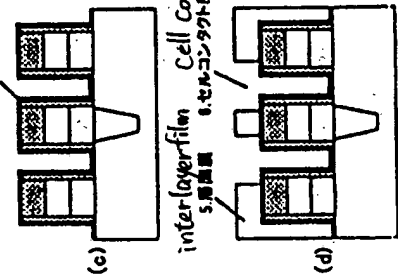


cell contact plug

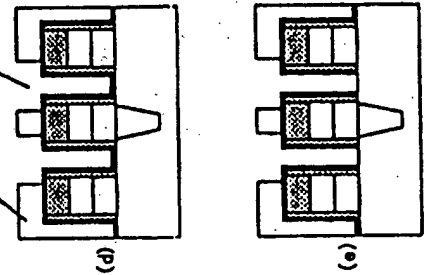


实施例④

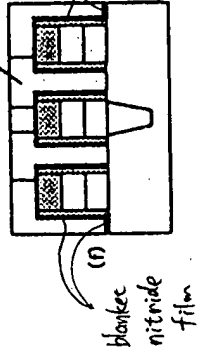
blanket nitride film
イ. プランケット窒化膜



interlayerfilm Cell Contact
5.層間膜 0.セルコンタクト部 Section

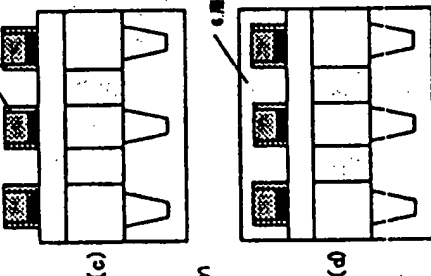


cell contact plug:
セルコンタクトプラグ

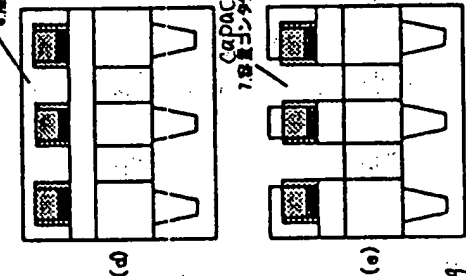


1. 大田コンダクト

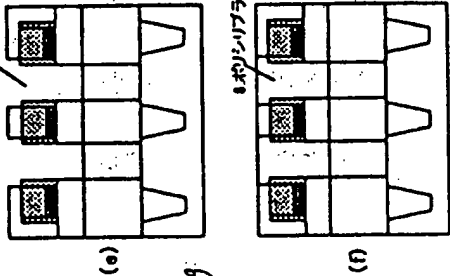
S. 望光器サイドウォール
nitride-film



interlayer

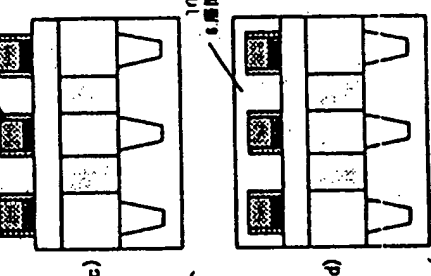


capacitor contact section
1. 容量コンタクト部

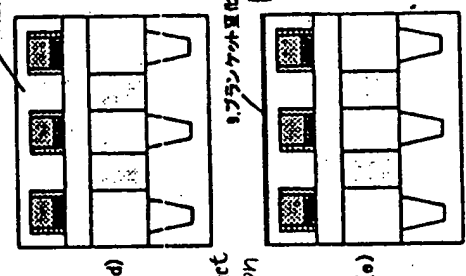


ポリシリコン poly silicon

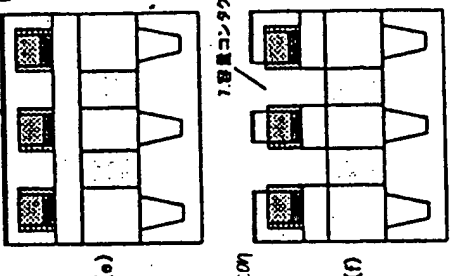
窒化膜サイドウォール nitride film



interlayer

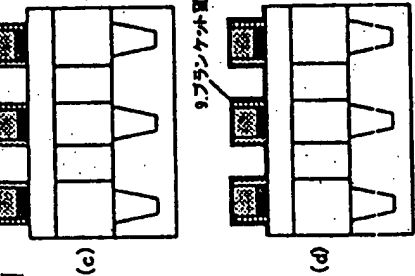


9. プランケット変位器

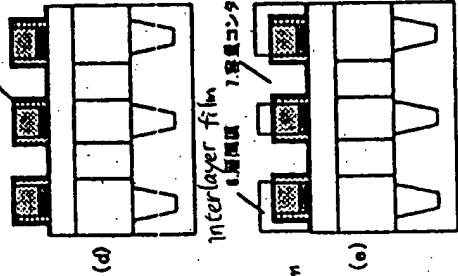


7.容量コンタクト部 / capacitor

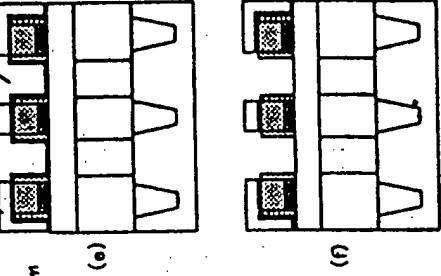
nitride film
side wall

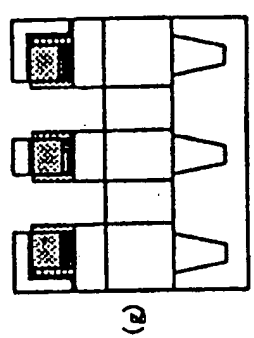
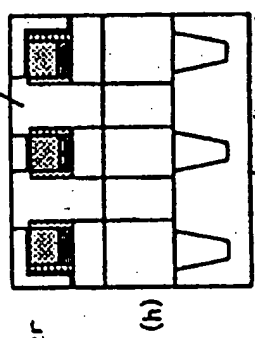
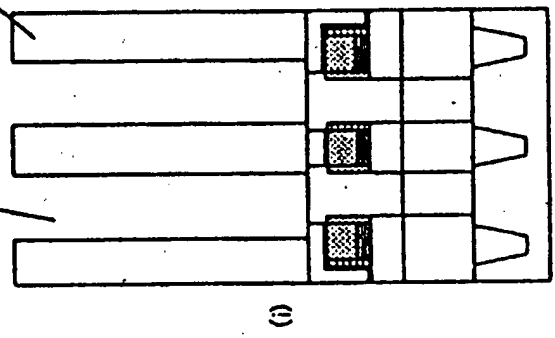
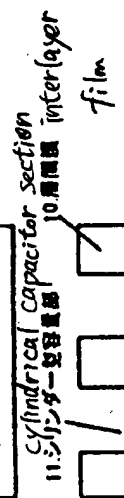
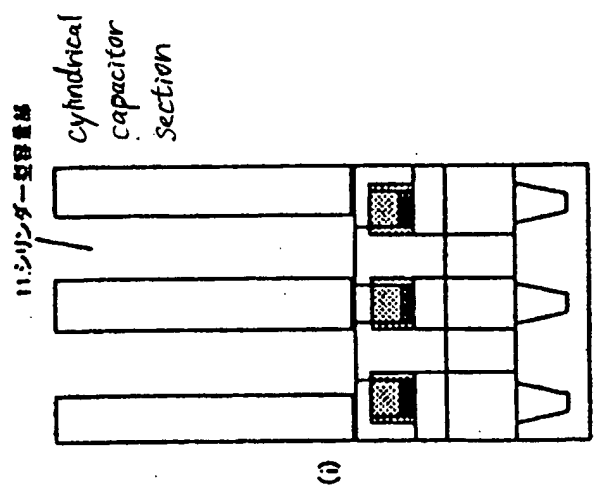
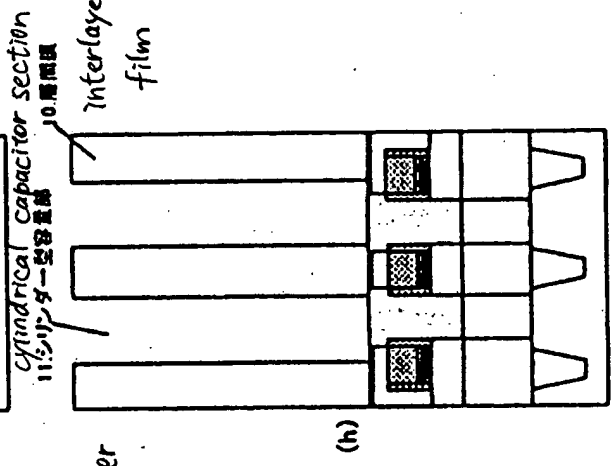
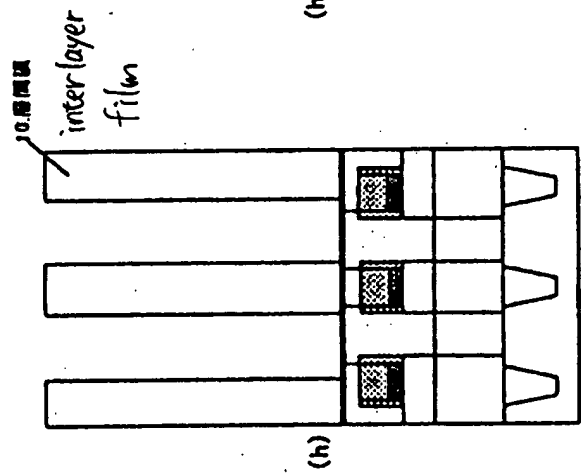
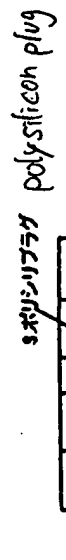
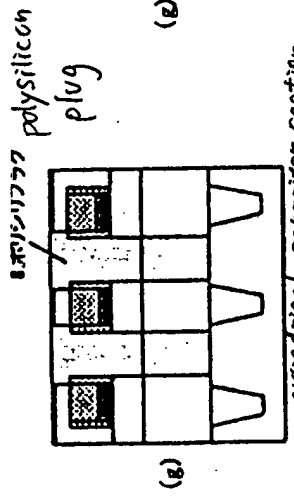
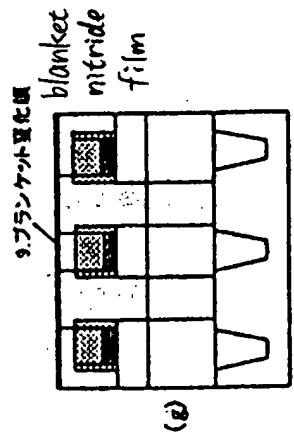


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Capacitor





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